Advantages and Challenges Associated with the Introduction of 450mm Wafers

(A position paper report submitted by the ITRS Starting Materials Sub-TWG)

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Introduction

Conversion to 450mm diameter can only occur if the economic advantages can be demonstrated for the entire supply chain. In previous diameter conversions, chip makers have not been overly concerned about the effect of the conversion on silicon wafer manufacturers. The change to 450 mm wafers, however, may be significantly different because of the magnitude of the financial burden placed upon the wafer producers. The extent of this burden will be estimated later in this paper, and some of its consequences will be explored.

Historical Perspective

The case for 450 mm wafers is based upon the economics of semiconductor chip production, and in particular, upon the growth rate of semiconductor chip demand. From the standpoint of a chip manufacturer, the driving forces for increasing wafer size from 300 mm to 450 mm will be the same as for earlier wafer diameter increases. Briefly stated, this is because the rate at which silicon is consumed (millions of square inches of silicon per year, MSI), and the corresponding rate at which wafer fab capacity must be increased, is a Moore's Law exponential that is interdependent with other factors that affect the semiconductor chip business. At some point along the growth curve for chip demand, it will become more economical for chip makers to build one 450 mm chip factory than two 300 mm chip factories. The exact timing for each company will depend on general macroeconomic conditions and the specific market context for that company, but competitive pressures will ensure that successful companies will make the diameter conversion at approximately the same time.

Fig 1 shows the production volume of silicon wafers in MSI, from 1973 through 2004. The volume is plotted on a logarithmic scale, with the least-squares best fit shown. There are several features of this graph to be

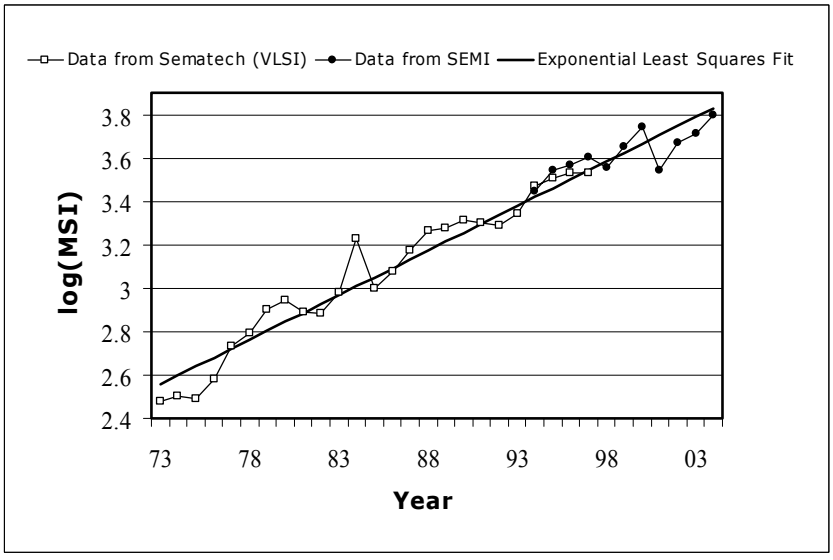

Fig. 1: Wafer Shipments, Millions of Square Inches (Worldwide; All Types of Silicon Wafers).

discussed, but first it should be noted that the fundamental reason for this phenomenal growth in silicon consumption is that Moore's Law allows an increasingly large amount of functionality to be placed on each chip. Increased functionality per chip has, historically, created a larger demand for chips, requiring a higher chip-production volume, so wafer fab capacities must correspondingly increase and wafer production is required to keep pace. For about the last twenty years, CMOS feature size shrinkage has been the enabling factor for staying on Moore's Law. However, *any* technology that increases functionality per chip will have a similar effect (assuming functionality is the limiting factor), and as long as chips are made on silicon substrates, demand for them (and for the silicon wafers used to make them) will continue to increase.

It is obvious from Figure 1 that the silicon wafer market has a cyclical aspect, and there are many years with excursions from the trend line that are quite pronounced. Nevertheless, the overall trend is clear: silicon consumption increases with a long-range compound annual growth rate (CAGR) of approximately 10%, which equates to a doubling in volume about every 7.4 years. The reason for the cyclical pattern is the same as the reason for periodic overcapacity and under-capacity in the semiconductor industry— imperfect market forecasting. Chip makers keep their silicon inventories too high when it is mistakenly believed that the market will continue to expand; then the purchase rate falls below normal as the chip makers' factories become under-loaded and wafer inventories are burned off. In process control terms, the pattern is a classic case of damped over-control.

The effect of macroeconomics can be seen more clearly by carrying the process control analysis one step further. Fig 2 shows the deviation of actual wafer shipments from the trend line, plotted as a control chart. The control zones (at +/- 1, 2, and 3 sigma) were determined using the moving range method for calculating control limits for individuals (ungrouped data). Recessions and other significant macroeconomic events are noted on the graph. The correlations to market activity levels are clear.

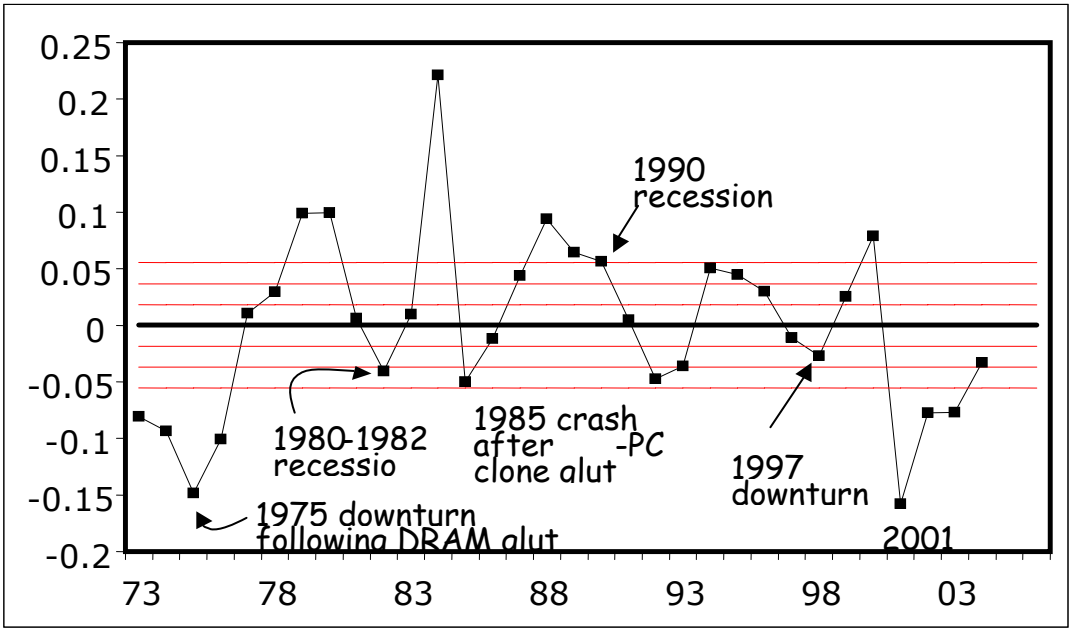

Fig 2: Actual Wafer Shipments Minus Trend Line Prediction (Logarithmic Scale), Plotted as a Control Chart

Economic Considerations

From the above discussion and data, we can conclude that if historical trends continue, silicon wafer consumption will reach approximately 12.5 BSI (billion in^2/yr) by 2013, provided that a robust market environment exists at that time. By way of comparison, the actual silicon consumption rate for 2004 was 6262 MSI, and the trend line prediction was 6737 MSI[1]. In other words, the silicon volume can be expected to about double, less than a decade from now.

Continuation of past trends presupposes that Moore's law, and it's implications for driving the market, will be sustained in the interim. It also requires that the general economy maintains its historical long-term growth rate. If these conditions develop as expected, semiconductor companies competing in a global economy are faced with the choice of either doubling their total capacity within the next ten years, or losing market share. Most companies probably would not be comfortable with the latter and will attempt to achieve the former in the most efficient way possible. Wafer diameter increases are recognized as an important means for achieving this efficiency and have, historically be a key enabler. The following quote by Goodal et al [1] illustrates the point.

"When the wafer area increases by >2 times, but the cost of the new tool set *for the same number of wafer starts* increases by only 30-40% (which is typical), the cost per area decreases by 30-50% -- an annualized improvement of ~4% when wafer size changes occur about every 10 years." This and similar arguments, have been the traditional viewpoint of the semiconductor device maker. However, on the subject of 450mm wafers, there appears to be significant disagreement as to whether this model continues to be valid.

It is important to recognize that the *timing* of this productivity boost also is crucial. Semiconductor factories tend to become obsolete in about ten years. Semiconductor companies recognize that an increase in wafer diameter gives a phenomenal, 30-50%, decrease in unit area cost at a time when factory upgrades are needed for rapid deployment of challenging technologies into the marketplace. Therefore it is imperative for them to make timely investments in larger-diameter plant capacity.

One of the primary and less visible assumptions that have been used in economic model based trend prediction has been that the cost per sq inch of the silicon wafer remains the same (or in fact declines) as the wafer sizes increase. Wafer manufacturers have become more sensitive to this assumption, particularly following the "false starts" of the industry in the move to 300mm wafers which resulted in a consolidation in the wafer manufacturing segment as well as a near death experience for at least one major silicon wafer vendor. This experience, along with the disconnect between the actual cost scalability of the silicon wafer manufacturing process and the reality of wafer pricing, has left the wafer business in questionable health. Current projections, made at higher levels in the industry food chain, project that the industry will move to 450 mm diameter wafers over about the next half dozen years, and maintain the use of the same assumptions for cost per square inch of silicon. The reality is that the cost to make the larger wafers is in fact growing. As wafer diameters increase, several things affect the cost of manufacturing: pull rates must be reduced, utilization efficiency of the polysilicon starting charge is reduced, costs of pullers and associated facilitization increase, and wafer thickness increases. The later aspect is interesting in that one can talk about the cost per cubic inch of silicon instead of the cost per square inch, since this is what matters to companies making the silicon wafers.

It is clear that the silicon wafer manufacturing industry, in its present marginal health, will not be able to support the move to larger diameter wafers under the same condition that have existed in the past: (1) little or no help form the rest of the industry in funding the development and transition and (2) the continued assumption that cost per square inch does not increase. Further it is likely that the cost of the wafers, especially with requirements for use of engineered substrates (epi, strained silicon, SOI, etc.) will become an increasing portion of the overall cost structure.

[1] As a sanity check, we note that for 2003 and 2004, the ratio of actual to projected MSI can be used to get a crude estimate of worldwide semiconductor manufacturer factory utilization. These numbers are 84% and 93% for 2003 and 2004, respectively, which seem reasonable.

The nature of the 450mm starting wafer

Polished CZ wafers will be, presumably, the starting form for T/M wafers, and the fundamental building block for other wafer types. The suggested [2] standard thickness for 450mm wafers is 825µm. The historical trend for wafer thickness is shown in fig 4. While, in principle, the wafers could be made thinner, such action would almost certainly lead to higher breakage during handling in manufacturing lines and significant issues with sagging during processing and measurement.

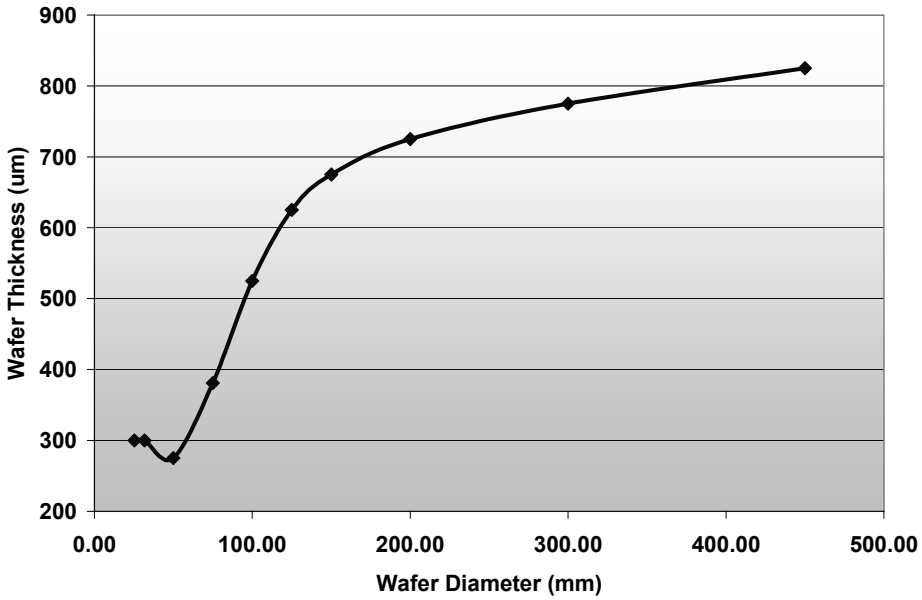

Fig 3: Wafer thickness trends with diameter

The introduction of 300mm drove some standardization of edge, notch and lasermark characteristics, 450mm must do even more. Standardized edges and replacement of the notch by a fiducial lasermark could help reduce cost of the starting substrate without loss of functionality. Two dimensional barcode marking can accommodate significant information useful for manufacturing lot tracking and, given the high final value of a fully processed 450mm wafer; it makes sense to use this technology to its fullest.

In most cases, 450mm will only be used for leading edge, high volume production. Presumably high yielding device lines will be required in order to justify the transition to 450mm. COP free defect engineered substrates, tightly controlled mechanical and electrical specifications will be standard. Application specific, multiple layer epi structures, graded layers; strained layers with choices in crystallographic orientations are likely to be required.

In principle, epitaxial wafers could be made but achieving the required thickness and resistivity uniformity would be more challenging. A new generation of epi reactors would be required and challenges of heat uniformity and gas distribution over large areas without slip formation would need to be carefully engineered. It is likely that such reactors would have lower throughput compared to smaller diameter machines.

SOI or some other solution to off-state leakage problems will be a necessity for leading edge performance devices. If there is sufficient cost advantage in making such devices on 450mm SOI then the driving force will be present. Any detailed cost model for 450mm wafers would also have to consider the economic viability of these advanced substrates.

There are no immediately obvious, fundamental technical barriers to the development of 450mm but there are clearly some issues that need to be addressed and some of these are considered next.

The technical challenges of 450mm wafer development

Crystal growth

There are no fundamental barriers to growing 450mm crystals but significant development work is required in order to determine the process windows through which the required quality parameters can be achieved. Crystallization by the Czochralski method, involves the controlled removal of heat from a melt. As the melt gets larger the time to remove the heat increases and the manufacturing throughput is lowered.

It is difficult to discuss cost and yields because intense competition in the supplier industry means that silicon suppliers are not willing to reveal details of their processes. However a simple, generic, model for CZ crystal growth can reveal some interesting trends as crystal diameter increases.

A normal practice for CZ growth, in order to achieve a full dislocation free crystal, involves growing a neck, a crown, the body of the crystal and then a tail or end-cone as shown in fig 3. The body is grown slightly over diameter so that, later, the peripheral 3-5 mm are removed by accurately grinding to the required diameter, thus providing a very tight distribution of finished wafer diameter. The shaded areas in Fig 3 show the silicon removed during these initial cutting and shaping processes and which contribute to the crystal yield losses. Using a simple model we can estimate the theoretical crystal yield. We can approximate the crown and end-cone parts by conical masses with the angle between the basal plane and side estimated (from published photographs) at 30 and 75 degrees respectively. (In practice the geometry is a little more complex but this serves as a first order approximation) Similarly, we can estimate the weight of pot scrap at 6% of charge weight and assume the crystals are grown 5mm over diameter (a conservative figure). Precise numbers may vary in practice but this approach (see fig 5) gives us a first approximation.

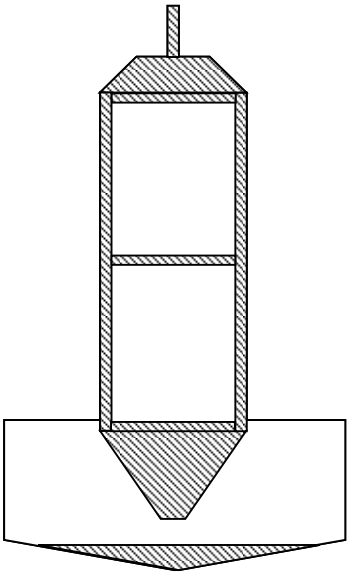

Fig 4: Yield losses in CZ Crystal Growth

Kerf losses during wire sawing are another significant source of material loss. Further losses occur downstream; silicon removal during grinding, etching and polishing operations, obviously scale with increasing area. In fact, by the time the silicon is in finished wafer form, as much as 30-40% of the starting charge is recycled (e.g. crown and end-cones) or scrapped (e.g. pot scrap, kerf losses).

	Wafer Diameter				
	100mm	***150mm***	***200mm***	***300mm***	***450mm***
As-Grown Diameter (mm)	103	153	205	305	455
As-Grown Cross Section (cm^2)	83.3	183.9	330.1	730.6	1626.0
Final Cross Section	78.5	176.7	314.2	706.9	1590.4
Crown Weight (Kg)	0.2	0.6	1.5	5.0	16.6
End Weight (Kg)	1.2	4.1	9.8	32.3	107.2
Pot Scrap (Kg)	2.4	6	9	19.2	60
Charge Weight (Kg)	40	100	150	320	1000
Typical Length (cm)	186	208	169	155	215
Grinding Losses (Kg)	2.1	3.5	6.2	8.6	17.8
Total Crystal Losses (Kg)	5.9	14.2	26.6	65.1	201.6
Crystal Yield (Kg/Kg)	85%	86%	82%	80%	80%

Fig 5: A simple generic model for CZ crystal yield

In order to approach theoretical crystal yields of the model, larger hot zones will be required although current hot zones may suffice for initial experiments. Fig 6 shows the variation of theoretical yield with charge size developed from the simple model. Typical operating conditions achieve theoretical yields (kg of grade one crystal per kg of starting charge) in the 80-90% range. In order for this to be achieved with 450mm crystals the starting charge size will have to be in the region 1-2 metric tons. Clearly such operations are much larger than anything currently undertaken and this will require significant development and investment on the part of silicon wafer makers and their suppliers. In reality wafer makers may have to accept lower theoretical yields. Equipment costs will be high and systems will need new considerations not encountered with smaller crystal growers. New safety systems appropriate for such large systems, handling devices with higher weight capability, etc would all be essential. Also the value of the starting charge would be considerable. Some

suppliers may prefer to sacrifice yield in order to forego the cost of developing such massive crystal growers. See for example figs 8 & 9. The overall issue of polysilicon utilization is discussed in the next section.

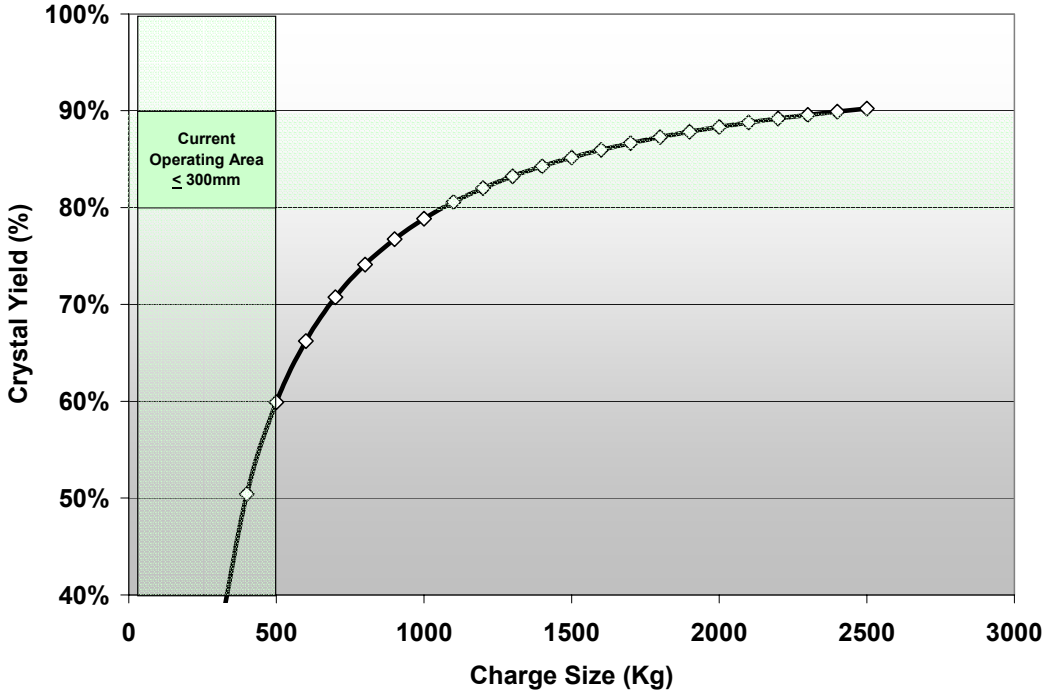

Fig 6: Variation of Theoretical Crystal Yield with Size of Starting Charge

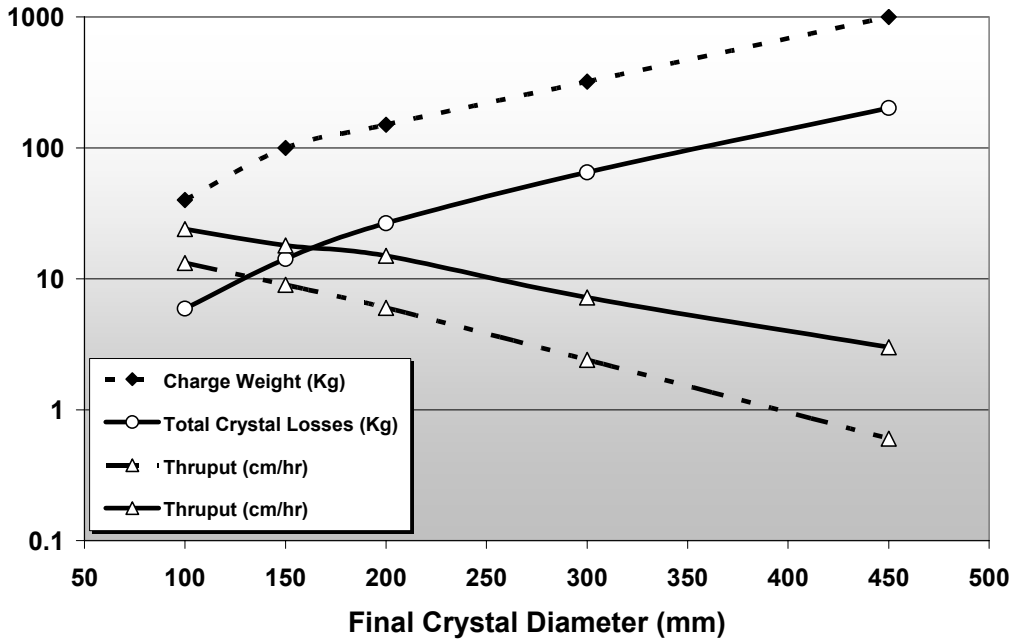

Fig 7: Variation of Crystal Throughput with Diameter

Poly utilization efficiency

Economical production of monocrystalline silicon in Czochralski (CZ) pulling requires increasingly large charges of polysilicon as discussed above and as shown through empirical data in fig 8 [3]. Larger charges require larger crucibles, which lead to yield losses due to larger residual melts even with optimal pulling process as depicted in fig 9. When crucible flaws or any other equipment malfunction led to dislocations, higher and by increasing diameters increasingly even higher yield losses could not be avoided. Consequently, manufacturing costs/cm² also increases (fig 10).

At present, poly utilization is about 0.55 g/cm² for semiconductor use. In 3-5 years, it may grow to 0.58 g/cm² with increasing ratio of larger diameter (300 mm) products. When larger than 300 mm products are requested, poly utilization may even grow to 0.6 g/cm². These values are empirical factors considering all the continuous improvement in manufacturing processes.

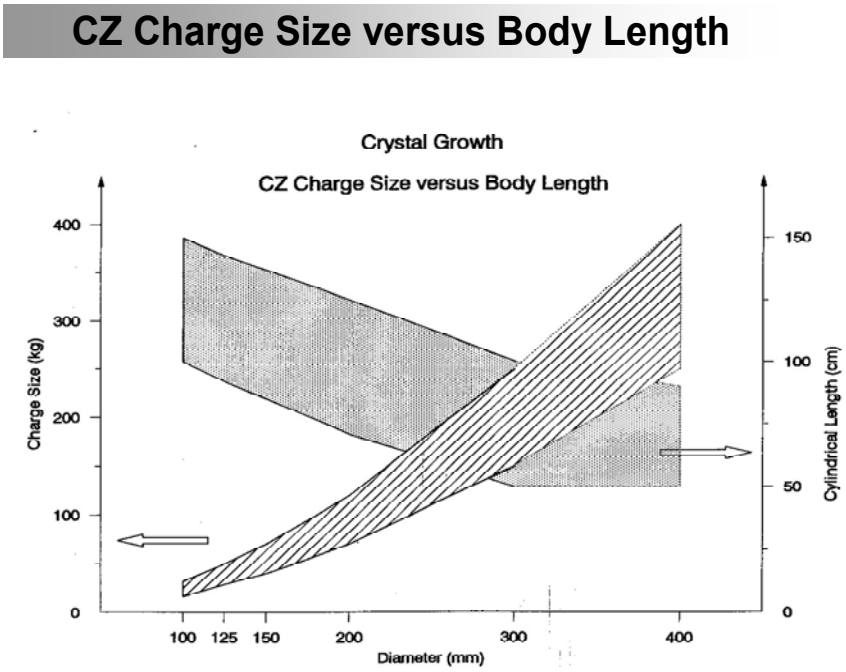

Fig 8: Economical conditions of manufacturing monocrystalline CZ ingots [3].

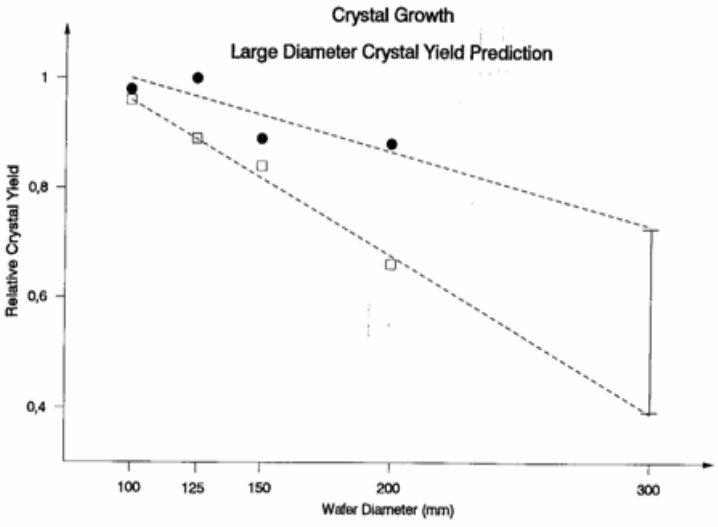

Fig 9: Maximum yields (dots) vs. wafer diameter, losses are due to increasing residual melts. Cut-back losses (squares) due to dislocations can further reduce the yield [3].

Today the solar industry consumes less than half of the world's poly production. However, according to conservative forecasting, the average growth (CAGR) of the semiconductor industry is about 6 %. Over the last 5 years, photovoltaic use of poly is increasing almost one order of magnitude faster than semiconductor use (fig 11). Specific estimates vary but within a few years more poly is forecast for solar energy use than for semiconductor use even when optimized specific silicon usage is applied [4]. Present demand for solar energy 1.5 – 1.7 GW would require more polysilicon than available today. Conservative forecasts predict demand for photovoltaic energy systems in the range of 2.5 GW i.e. ~25,000 tons/year by 2010. However, 5 GW (~50,000 tons/year) has been predicted when China and California also start developing photovoltaic industries. The solar-poly market is, currently, characterized by an obvious supply gap. Solar customers are securing supply in long-term contracts. The growing demand cannot be met without the addition of new poly fabs.

A new poly fab with a capacity of 3000 – 5000 tons/year can be built in 2-3 years on a green field site, increasing demands for semiconductor-poly, due to introduction of larger diameter wafers (>300 mm) must be announced in good time and the mutual commitments between suppliers and customers of semiconductor-poly will need to be guaranteed in a similar manner to the solar-poly market.

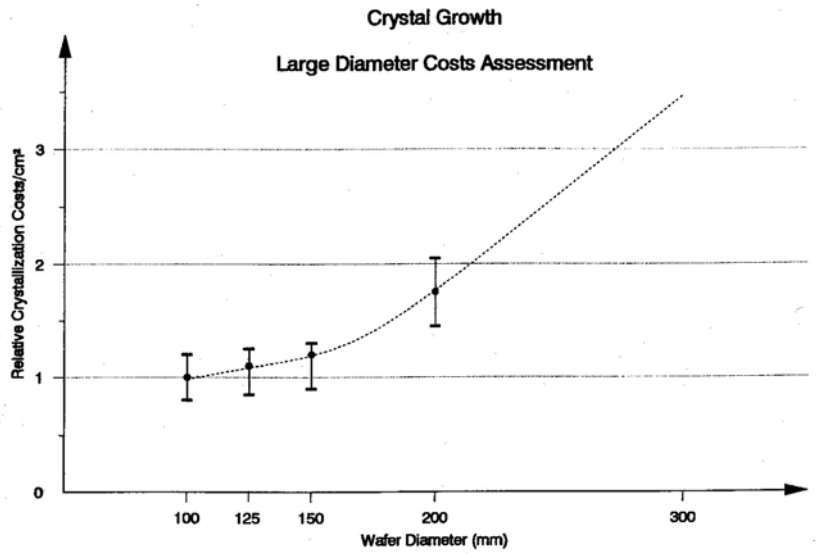

Fig 10: Cost effects of increasing wafer diameter [3].

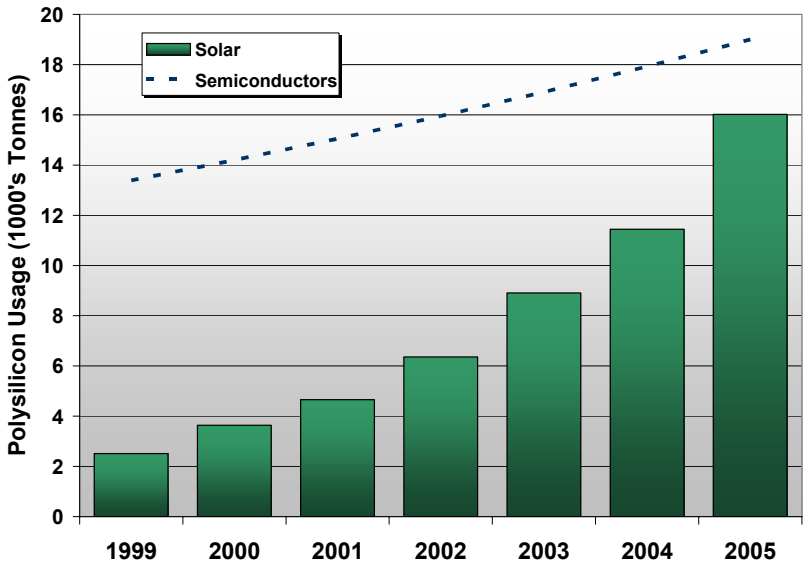

Fig 11: Polysilicon Usage by the Solar Industry

Wafering

While there do not appear to be any fundamental barriers to converting 450mm crystals to wafer form, the challenges will hold a greater level of complexity. In principle, wire saws can be scaled to cut 450mm and the key issues will be, as with smaller diameters, control of TTV and warp. Increasing diameter leads to larger components in the machine bed and greater issues with wire and pulley wear, temperature control and handling of larger, heavier ingots. While these issues are not insurmountable, solutions will add to the cost of the tool.
The increased drag on the wire due to the longer cut length may effect the lower limit of wire diameter which can be used and therefore impact the kerf loss. Wire wear will increase and potentially limit the TTV of as-cut wafers. Wire development will need to continue to solve this problem.
Similarly, downstream processing will require larger machines and most of these would be automated, cassette to cassette operation. Whatever the removals are in 300mm, the scrap for 450mm will be approximately twice that in volume terms. (Assuming same kerf and depth of machine removal but twice the wafer area) Downstream processing tools will also need to be developed and again there will need to be a suitable financial incentive (ROI) for the developers.

Thermal processing for epi, annealing and similar steps will require significant work. Supporting larger mass wafers without inducing slip will be a challenge. Innovative solutions will be required.

SOI will inevitably need a longer lead time since development is limited by starting wafer availability. Again process equipment development, especially ion implanters, will require an appropriate financial incentive. Bow/warp issues in SOI (and other composite wafers, such as p/p+ epi and SiGe heteroepi) due to thin film stresses will add additional complexities to the problem. Even longer lead times are likely for more exotic wafer types – SSOI, GeOI, etc

While the advantages of larger wafer for semiconductor device makers are well known, those advantages do not apply for wafer makers. When a defect occurs in semiconductor device manufacturer's line so as to create a defective square inch of silicon, the defective area is easily discarded. Counting the cost per square inch of silicon makes sense. The wafer make however sees a different story. A defect on one square inch of silicon means discarding the entire wafer. The larger the wafer, the larger the cost of yield loss. This is equivalent to a manufacturing line with a very large batch size. When it works, the line can be very efficient when a batch fails, due to some unforeseen variation in the process, the cost of yield losses can be huge. The device industry made moves toward single wafer processing because this offered advantages for short cycle times and fast feedback loops, lower WIP and less material at risk. As the wafer size gets bigger, we force the wafer maker in the wrong direction. As mentioned previously, in order to achieve commensurate crystal pulling yields at 450mm diameter, starting charge sizes need to be in the range of 1-2 metric tons. At around $40/kg for poly silicon this means a starting charge cost in excess of $40,000. This does not include the cost of the crucible. Throughout the wafer finishing process the larger the wafer the greater the vulnerability to a killer defect and the subsequently larger yield losses. Any detailed economic model for a diameter change must include this effect and its impact on wafer cost.

The economic challenges of 450mm wafer development

Given that there do not appear to be any fundamental *technical* barriers to the development of 450mm diameter wafers, the heart of the matter is an economic concern. The question is simple: 'Is there sufficient economic incentive at all levels of the supply chain, to invest in the development of 450mm substrates for the semiconductor industry?' The answer, of course, is much more difficult.

While it is generally accepted that larger diameters have the potential for manufacturing more chips per wafer which lowers the cost, this is offset by the increased complexity in manufacturing and handling larger wafers and the concomitant toolset. Extrapolation of historical trends, show that, a 22nm fab line could cost in excess of $10B. (300mm predictions were much too low. A better job must be done for 450mm). Such large investment requirements would surely limit the number of participants unless a new approach can be found.

Suppliers to this market segment would also incur heavy development costs but with only a very limited number of customers. It is likely that suppliers would find it difficult to earn a significant return on the cost of development.

The question arises, is 450mm an attractive proposition for chip makers if they have to bear a significant part of the supply chain investment burden themselves. Is the development cost too high for any one company to absorb? If so, what alternative funding structures could be devised to make it palatable? Could partnerships be the most likely route for success?

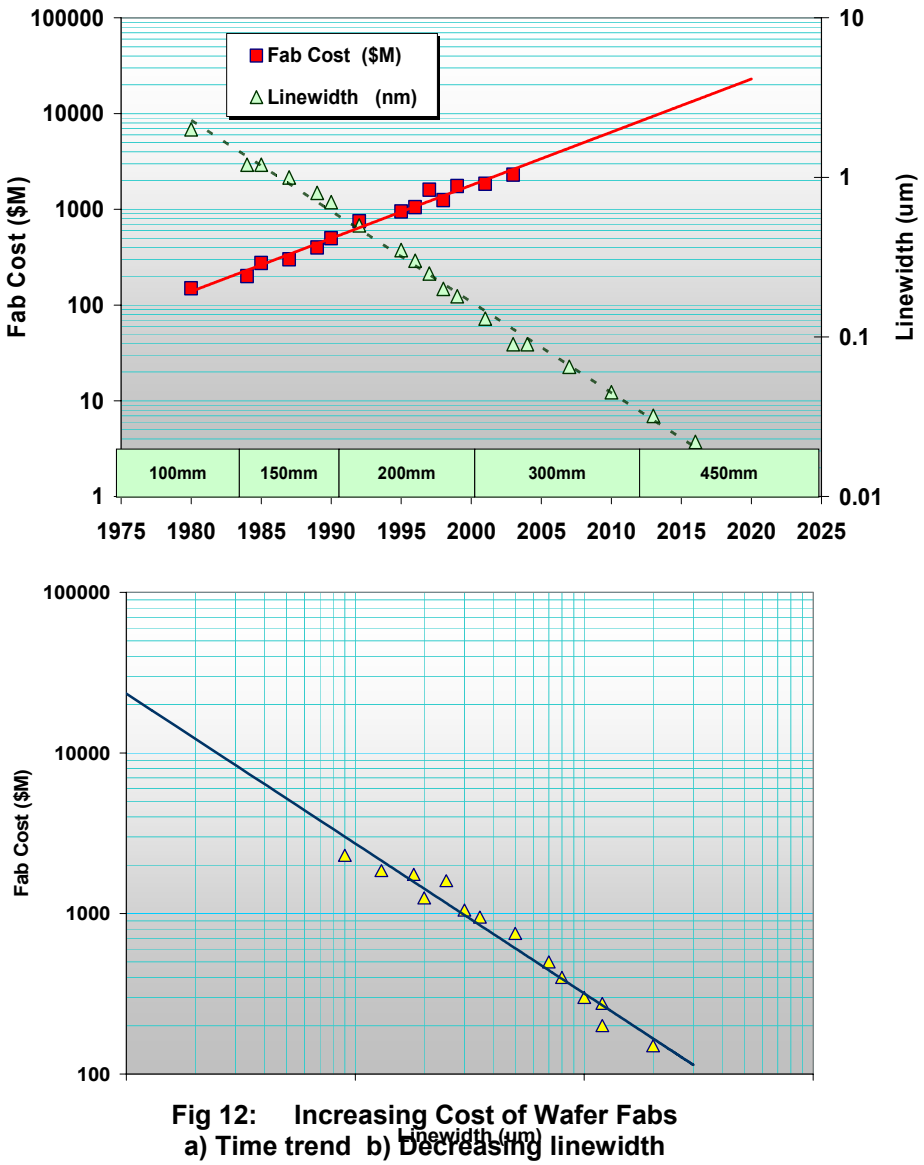

Fig 12: Increasing Cost of Wafer Fabs
a) Time trend b) Decreasing linewidth

In order to resolve the issue a detailed model has to be developed. The model must represent the real situation for each element in the supply chain. It must show clearly that such a development makes sound business sense for all elements, then and only then will a successful diameter change be implemented.

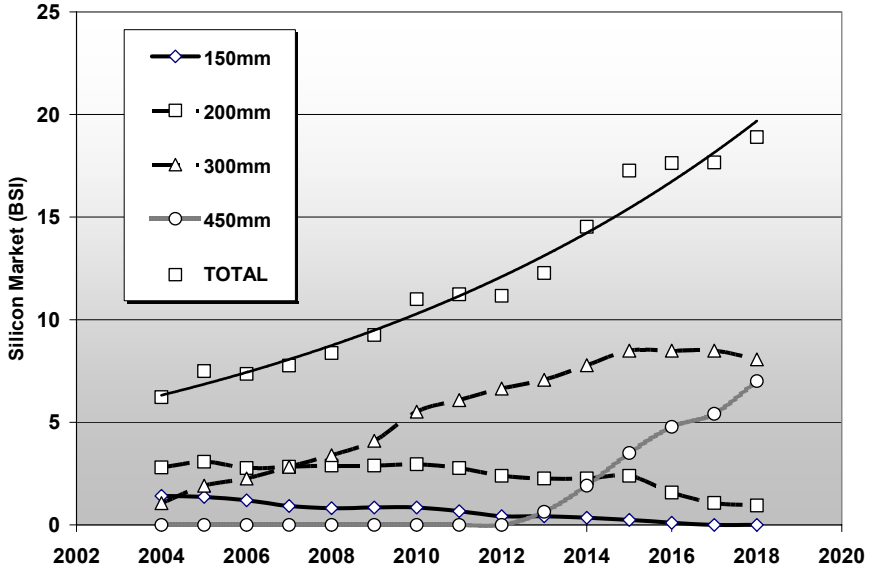

Fig 13: Market Forecast by Diameter (After [5])

The market forecast is shown in fig 13. Simple business scenarios can be devised in order to estimate the likely payback time for an investment in 450mm. The table in fig 14 shows two sets of assumptions for Average Selling Price (ASP), margin as a percent of sales revenue and spending as a percentage of year on year incremental revenue. Further assuming a lead time of 3 years from start of development to product launch, a set of low and high assumptions are used in conjunction with the revenue numbers from fig 13. A simple model is then used to generate the chart in fig 15.

	Low (1)	**High (2)**
ASP ($/Sq. In.)	$1.2	**$1.5**
Margin (%)	10%	**50%**
Spending (%)	**15%**	**25%**

Fig 14: Table of assumptions for chart in fig 15.

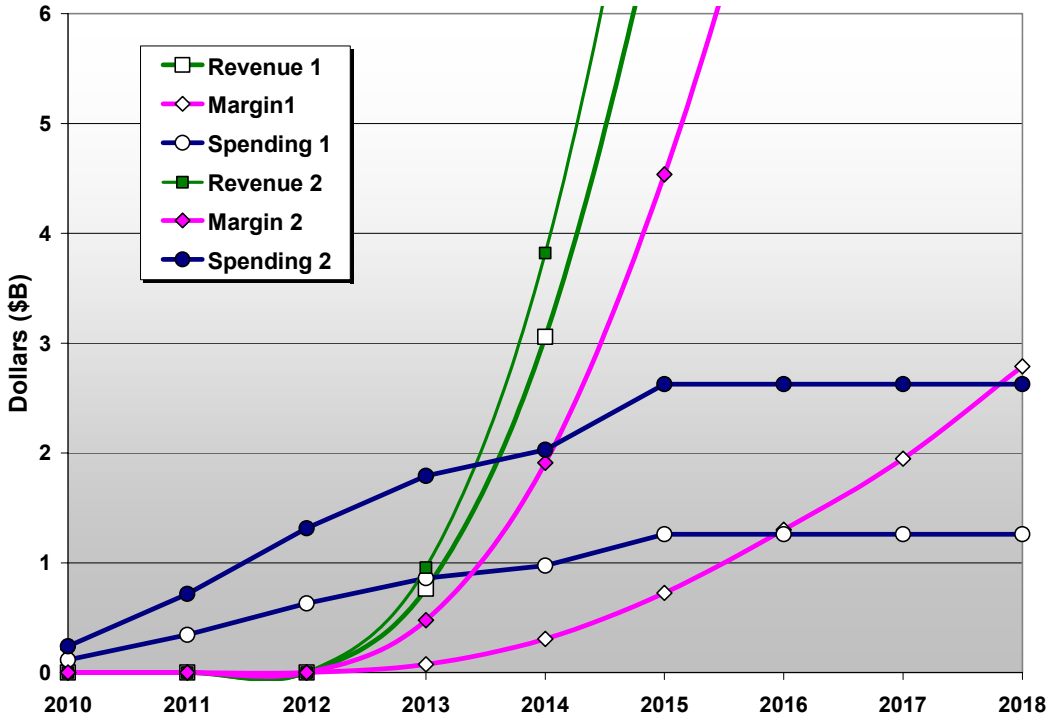

Fig 15: Payback Estimates for a 450mm Project

When cumulative margin in fig 15 exceeds cumulative spending the investment starts to have a positive payback. Using the assumptions of fig 14 the payback time could range from 3-8 years with a more probable range of 4-6 years. This is assuming that the required market volume can be met with a total investment of $1.3B and $2.6B. While this situation is obviously oversimplified one can start to see the difficulty for wafer manufacturers. Many factors can erode margins in any business. In the case of 450mm wafer manufacturing we are pushing into the realm of higher yield losses relative to smaller diameters and heavy investments in order to meet the technical challenges. The risk of such a venture is considerable.

Summary

In summary, it appears that, the introduction of 450mm wafers will require significant effort to achieve consensus within the industry as to the economic viability of such substrates. While, from a technical point of view, there do not appear to be any fundamental barriers, engineering challenges will be significant. Large crystal growers, handling systems, new safety considerations, wafer handling equipment and automation systems will require a significant design effort beyond mere scaling of earlier equipment generations. Semiconductor grade polysilicon shortages and unprecedented competition from the solar industry will ensure that the efficiency of polysilicon usage becomes an issue for the semiconductor industry. Uniformity of wafer parametrics over 2x the area will present further challenges for wafer and device manufacturers and their equipment suppliers.

Throughout the industry there is considerable doubt as to the economic viability of meeting these challenges and that is enough to slow down or perhaps even prevent the introduction of 450mm wafers. At a time when the industry is facing increasing divergence in material solutions it is unlikely that wafer manufacturers will invest readily in 450mm development. At the very least, detailed engineering cost models will need to be developed that are understood and agreed to by the entire supply chain.

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